(f) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

R E M A R K S

Claims 2 and 6 have been slightly amended to make the language clearer.

Claims 1-17 were rejected under 35 U.S.C. 102 in view of Wang.

The Patent Office, in rejecting claims 7-9, states that Wang discloses means connecting bit line to sense nodes for imperfectly isolating sense nodes from the bit line (page 2, second last paragraph of office action). Applicant, in the second last and last paragraphs on page 4 and the continuation of the paragraph at the top of page 5 of the amendment letter dated March 22nd, 1993 pointed out that these claims do not claim what the Patent Office states is taught in Wang. Applicant does not understand what set of claims the Patent Office may be using, since the aforenoted claims in applicant's set of claims do not contain those limitations. It would be appreciated if the Patent Office would check its claims and telephone the undersigned and advise whether claims 7-9 (as well as claims

6 and 10) contain the "isolating means" limitation in its copy.

If it does not contain that limitation, clearly the rejection under 35 U.S.C. 102 of claims 7-9 is unwarranted, since there is no basis for the rejection. Withdrawal of the rejection and allowance of claims 7-9 are respectfully requested.

The Patent Office has rejected claims 1-17 over both Wang and Miyamoto et al for the reason that the Patent Office considers that all field effect transistors (such as the isolating transistors 14 in Wang) are imperfect and leak current, and thus conform to what is defined in applicant's claims. The Patent Office has concluded that there is leakage in the transistors of the references with no evidence given which could be argued by the applicant. The Patent Office is requested to provide evidence that a current can leak through a semiconductor switch, that this is a characteristic of most transistors in the market today, and that this would not make the references inoperative.

Wang, for example, clearly specifies that transistor 14 is an isolating transistor. If it leaked current, it would not perform the function of isolation. Thus the Patent Office has attributed characteristics to the pertinent critical elements of Wang, and Miyamoto et al which operates in a manner similar to Wang, which are directly contrary to what is taught in those references and

which would render those elements inoperable to perform the function described in those references.

The Patent Office states that the prior arts did not fully admit that their transistor switches are "perfected isolators". By this reasoning the Patent Office would consider that a table top which is described in a patent as being hard, as being imperfectly hard when considered at the atomic level, which clearly would be an illogical conclusion to a reasonable person.

The isolating transistors in Wang and Miyamoto et al work because if there is any leakage through them, it is for all intents and purposes negligible. The present invention, on the other hand, works because current leakage is not negligible.

Accordingly, it is submitted that to a reasonable person skilled in the art, an isolating transistor would be considered for all intents and purposes isolating with negligible current leakage. Claims 1, 16 and dependent claims of the present invention which have defined imperfect isolators, would clearly be considered as passing leakage current which is not negligible. To consider that the isolating transistors of Wang and Miyamoto et al are imperfect isolators for the purposes described in those references is clearly directly contrary to their teachings, and to attribute "imperfect isolating transistor" to "isolating transistor" in those references, after reading

and understanding those references, defies what is taught in those references.

It appears to the applicant that the critical issue before us is whether the claims can be interpreted as intended by the applicant. It is believed from the comments of the Patent Office that it has an accurate understanding of the invention. Therefore in an effort to resolve the issue applicant has made an effort to amend the claims in order to make more definite the language defining the leakage characteristics of the imperfect isolating means and function.

As described on page 3, lines 17-25, the gate of the FET isolation means in applicant's invention is held at a voltage which maintains it imperfectly open, and changes to a level which allows each device to conduct when the sense amplifier operates. As applicant has defined on page 3, lines 22-25, imperfect isolation referred to in the present application means that the source-drain of the FET is in a high resistance state, but allows some charge leakage through it. Thus an enabling voltage causes the imperfect isolating means to leak current through it.

Claims 2 and 4 define the imperfect isolating means as being field effect transistors, and claims 3 and 5 define the voltages applied to the gates of the field effect transistors as being of particular level to provide the voltages for causing current leakage through the FETs.

Applicant has amended claim 1 to bring some of the characteristics defined in claims 3 and 5 into claim 1, i.e. that the imperfect isolating means is a high resistance controllable current leakage imperfect isolating means for receiving an enabling voltage for causing current leakage therethrough. Claims 3 and 5 have been slightly amended to conform the terminology.

It is believed that with these amendments, the language defining structure and operation of the imperfect isolating means has been more clearly distinguished from the isolating transistors of Wang and Miyamoto et al.

In the event that the Patent Office considers the claims still not patentable, entry of the amendments for the purposes of appeal is respectfully requested.

The reason that the amendment was not earlier presented is that the subject matter was already claimed in at least claims 3, 5 and dependent claims, and it was not deemed necessary to amend claim 1 accordingly, since it was clear that the defined voltage levels of the voltage source applied to the gates of each field effect transistor would produce the desired enabling effect of causing current leakage, which is not found in the references.

Claim 6 defines in clause (e) a pair of field effect transistors, one being a P-channel enhancement mode type and the other being an N-channel enhancement mode type connected in a particular relationship with other elements in the claim. Nothing in any way similar is described in

the references, and the Patent Office has found or pointed out no corresponding elements, nor combinations as defined in that claim.

Claim 10, and other claims dependent from claim 1, defines in clause (c) a pair of field effect transistors, one having its source-drain circuit connected between the restore enable input and the high logic level power supply voltage and the other having its source-drain circuit connected between the sense enable input and the low logic level power supply. Nothing similar is described in any of the references.

Withdrawal of the rejection of all of the claims and allowance of this application are respectfully requested.

If the Patent Office considers that there are matters remaining that could be resolved by telephone interview, the Examiner is invited to telephone the undersigned at (202) 828-0300.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (628.30050X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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